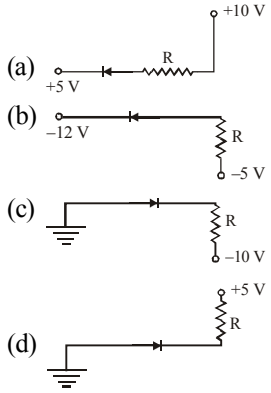
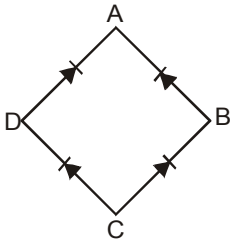
28 Semiconductor Electronics : Materials, Devices and Simple Circuits

Diagram Based Questions :

1. Of the diodes shown in the following diagrams, which one is reverse biased ?

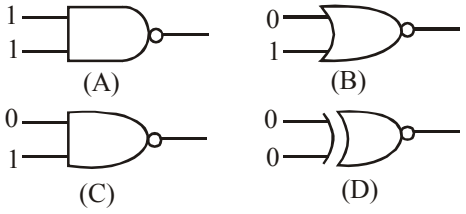


2. In bridge rectifier circuit, (see fig.), the input signal should be connected between



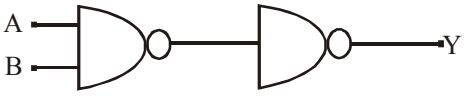
(a) A and D (b) B and C
(c) A and C (d) B and D

3. Which of the following gates will have an output of 1?



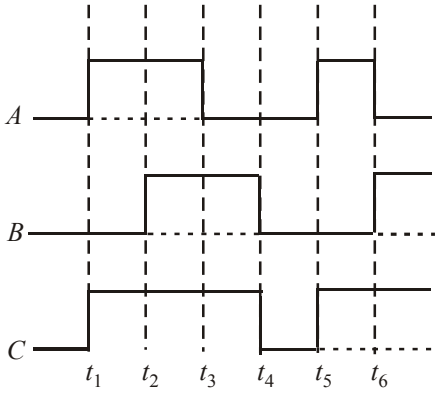
(a) D (b) A
(c) B (d) C

4. Following diagram performs the logic function of



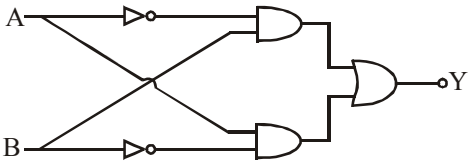
(a) XOR gate (b) AND gate
(c) NAND gate (d) OR gate

5. The figure shows a logic circuit with two inputs A and B and the output C. The voltage wave forms across A, B and C are as given. The logic gate circuit is:



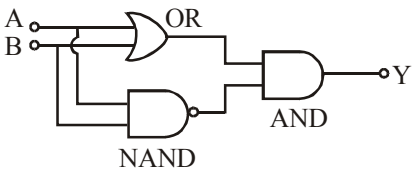
(a) OR gate (b) NOR gate
(c) AND gate (d) NAND gate

6. The following circut represents



(a) OR gate (b) XOR gate
(c) AND gate (d) NAND gate

7. The following configuration of gate is equivalent to



(a) NAND gate (b) XOR gate
(c) OR gate (d) NOR gate

Solution

1. **(d)** Positive terminal is at lower potential (0V) and negative terminal is at higher potential 5V.

2. **(d)** The input signal should be connected between two points of bridge rectifier such that in positive half wave of input signal, one p-n junction should be forward biased and other should be reverse biased and in negative half wave of input signal, the reverse should take place. It will be so when input is connected between B and D.

3. **(d)** (A) is a NAND gate so output is

$\overline{1\times1}=\overline{1}=0$

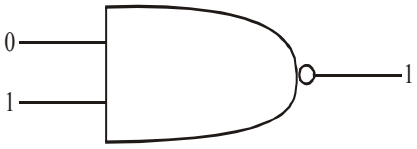
(B) is a NOR gate so output is

$\overline{0+1}=\overline{1}=0$

(C) is a NAND gate so output is

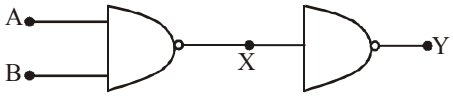
$\overline{0\times1}=\overline{0}=1$

(D) is a XOR gate so output is $0\oplus0=0$



Following is NAND Gate $Y=\overline{AB}$

4. **(b)**



$X=\overline{AB}$

$\therefore Y=\overline{X}=\overline{\overline{AB}}$

Y = AB by Demorgan theorem

$\therefore$ This diagram performs the function of AND gate.

5. **(a)**

A	0	1	1	0
B	0	0	1	1
C	1	1	1	1

OR gate

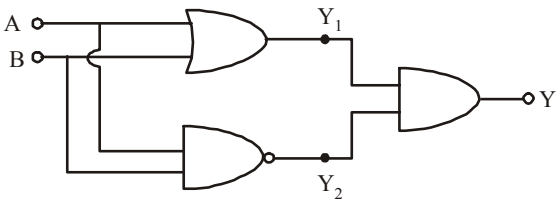
6. **(b)** Output of upper AND gate = $\overline{A}B$

Output of lower AND gate = $A\overline{B}$

$\therefore$ Output of OR gate, $Y=A\overline{B}+B\overline{A}$

This is boolean expression for XOR gate.

7. **(b)**



$Y_1=A+B,\ Y_2=\overline{A.B}$

$Y=(A+B)\cdot\overline{AB}$

$=A\cdot\overline{A}+A\cdot\overline{B}+B\cdot\overline{A}+B\cdot\overline{B}$

$=0+A\cdot\overline{B}+B\cdot\overline{A}+0=A\cdot\overline{B}+B\cdot\overline{A}$

This expression is for XOR